Click here for production status of specific part numbers.

MAX20046

Automotive Hi-Speed USB 2.0 Protector

General Description

The MAX20046 device provides high-ESD and short-circuit protection for the low-voltage internal USB data and USB power line in automotive radio, navigation, connectivity, and USB hub applications. The device supports USB Hi-Speed (480Mbps), USB full-speed (12Mbps), and USB low-speed (1.5Mbps) operation.

The short-circuit protection features include short-to-battery on the protected HVBUS, as well as short-to-HVBUS and short-to-battery on the protected HVD+ and HVD-. Short-to-GND and overcurrent protection are also provided on the protected HVBUS output to protect the internal BUS power rail from overcurrent faults.

The device features high-ESD protection to ±15kV Air Gap and ±8kV Contact on the protected HVBUS, HVD+, and HVD- outputs.

The device features a 500mΩ (max) USB power switch, and two low on-resistance (R_{ON}), USB 2.0 data switches. This device also features an enable input, fault output, 9ms fault-recovery time, 1ms overcurrent-blanking time, and integrated overcurrent autoretry.

The MAX20046 is available in a 12-pin lead-free, TQFN-EP package and operate over the -40°C to +105°C temperature range.

Benefits and Features

- Low 23mA/45mA (MAX20046GTCA/V+) or 60/120mA (MAX20046GTC/V+) Current Threshold for Module-to-Module and Peripheral USB Connections
- Targeted Features for Optimized USB Performance
  - Two R_{ON} 3.3Ω (typ) USB 2.0 Data Switches
  - 480Mbps, 12Mbps or 1.5Mbps USB 2.0 Operation
  - 9ms Fault-Recovery Time
  - 1ms Overcurrent Blanking Time
  - 5.7V (typ) Fixed HVBUS Protection Trip Threshold
- Robust for the Automotive Environment
  - Short-to-Battery and Short-to-GND Protection on Protected HVBUS Output
  - Short-to-Battery and Short-to-HVBUS Protection on HVD+ and HVD- Outputs
  - Tested to ISO 10605 and IEC 61000-4-2 ESD Standards
  - 12-Pin (3mm x 3mm) TQFN-EP Package
  - -40°C to +105°C Operating Temperature Range
  - AEC-Q100 Qualified

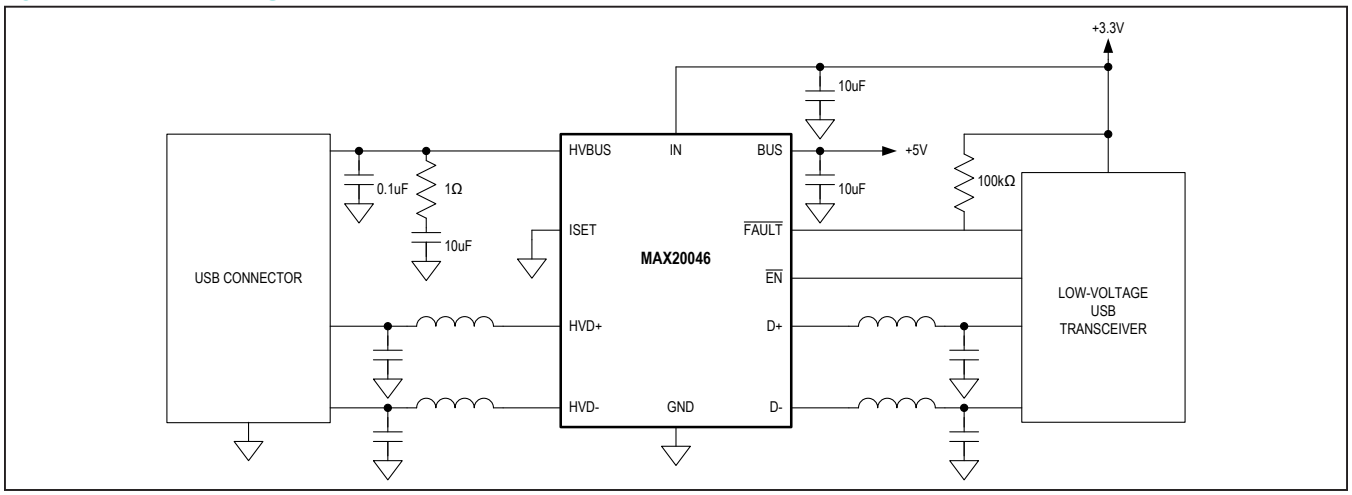
Applications

- Automotive USB Protection

***Ordering Information* appears at end of data sheet.**

***Functional Diagram* appears at end of data sheet.**

Typical Operating Circuit



Absolute Maximum Ratings

(All voltages referenced to GND.)
BUS, IN .....-0.3V to +6V
$\overline{FAULT}$, $\overline{EN}$, D+, D-, ISET .....-0.3V to +6V
D+, D- to IN .....+0.3V
HVBUS, HVD+, HVD- .....-0.3V to +18V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 12 TQFN	
Package Code	T1233+5C
Outline Number	**21-0136**
Land Pattern Number	**90-0019**
PACKAGE TYPE: 12 SW TQFN	
Package Code	T1233Y+5C
Outline Number	**21-100171**
Land Pattern Number	**90-100060**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	68°C/W
Junction to Case (θ_{JC})	11°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{BUS} = 5.0V V_{IN} = +3.3V, T_J = T_A = -40°C to +105°C. R_L = ∞, unless otherwise noted. Typical values are at $V_{\overline{EN}}$ = 0V or $V_{\overline{EN}}$ = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Range (BUS)	V_{BUS}		4.75		5.5	V
Power-Supply Range (IN)	V_{IN}		3.0		3.6	V
BUS Input Current	I_{BUS}	$V_{\overline{EN}}$ = 0V, no load, no fault (MAX20046GTCA/V+)			440	µA
		$V_{\overline{EN}}$ = 0V, no load, no fault (MAX20046GTC/V+)			500	
IN Input Current	I_{IN}	$V_{\overline{EN}}$ = 0V, no load, no fault			12	µA
BUS Undervoltage Lockout	V_{UVLO}	V_{BUS} falling (Figure 1)	3.85	4.2	4.55	V

Electrical Characteristics (continued)

(V_{BUS} = 5.0V V_{IN} = +3.3V, T_J = T_A = -40°C to +105°C. R_L = ∞, unless otherwise noted. Typical values are at $V_{\overline{EN}}$ = 0V or $V_{\overline{EN}}$ = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BUS ANALOG SWITCH						
HVBUS Protection Trip Threshold	V_{OV_BUS}	HVBUS rising (Figure 2)	5.5	5.7	5.9	V
Voltage-Protection-Response Time	t_{FP_BUS}	HVBUS rising (Figure 2)		0.4	1	µs
Protection-Recovery Time	t_{FPR_BUS}	HVBUS falling below V_{OV_BUS} (Figure 2)	6	9	11	ms
HVBUS Short-to-Ground Threshold	V_{SHRT}	Low-to-high transition (Figure 3) (MAX20046GTCA/V+)	0.75		1.35	V
		Low-to-high transition (Figure 3) (MAX20046GTC/V+)	1.0		1.75	
Short-to-Ground Response Time	t_{FPS}	HVBUS falling to GND (Figure 3)		0.3	1	µs
On-Resistance	R_{ON}	V_{BUS} = 5V	150	270	500	mΩ
Forward-Current Threshold (Note 2)	I_{THR}	Connect ISET to GND (Figure 4) (MAX20046GTCA/V+)	18	23	27	mA
		Connect ISET to 3.3V (Figure 4) (MAX20046GTCA/V+)	34	45	55	
		Connect ISET to GND (Figure 4) (MAX20046GTC/V+)	50	60	70	
		Connect ISET to 3.3V (Figure 4) (MAX20046GTC/V+)	105	120	135	
Overcurrent Blanking Time	t_{BLANK}	Figure 4	0.6	0.8	1.0	ms
Overcurrent-Retry Blanking Time	t_{BLANK_RETRY}	Figure 4		9		ms
Overcurrent-Autoretry Time	t_{RETRY}	Figure 4		132		ms
HVBUS Off-Leakage Current	I_{LKGOFF}	V_{HVBUS} = 18V, V_{BUS} = 4.75V			600	µA
		V_{HVBUS} = 18V, V_{BUS} = 0V, V_{IN} = 0V			800	
Thermal Shutdown				165		°C
Thermal-Shutdown Hysteresis				15		°C
USB DATA SWITCH						
Analog Signal Range			0		3.6	V
Protection-Trip Threshold	V_{OV_D}	HVD+, HVD- rises from V_{IN} to > V_{IN} +1V (Figure 2)			3.9	V
Protection-Recovery Time	t_{FPR_D}	HVD+, HVD- falling to below V_{OV_D} (Figure 2)	6	9	11	ms
Protection-Response Time	t_{FP_D}	HVD+, HVD- rises from V_{IN} to > V_{IN} +1V (Figure 2)		0.5	1	µs

Electrical Characteristics (continued)

(V_{BUS} = 5.0V V_{IN} = +3.3V, T_J = T_A = -40°C to +105°C. R_L = ∞, unless otherwise noted. Typical values are at $V_{\overline{EN}}$ = 0V or $V_{\overline{EN}}$ = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Resistance	R_{ON}	V_{BUS} = 5V, I_L = 40mA, 0 ≤ V_D ≤ 3.6V		3.3		Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_{BUS} = 5V, I_L = 40mA, V_D = 1.5V, 3.0V			0.25	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	I_L = 40mA, V_D = 0V or 0.4V			0.25	Ω
HVD+, HVD- Off-Leakage Current	I_{HVD_OFF}	V_{HVD+}, V_{HVD-} = 18V, V_{D+}, V_{D-} = 0V			20	µA
		V_{HVD+}, V_{HVD-} = 18V, V_{D+}, V_D = 0V, V_{IN} = 0V, V_{BUS} = 0V			20	
HVD+, HVD- On-Leakage Current	I_{HVD_ON}	V_{HVD+}, V_{HVD} = V_{IN}, $V_{\overline{EN}}$ = 0V			5	µA
On-Channel -3dB Bandwidth	BW	R_L = 50Ω, source impedance 50Ω (Figure 5)		864		MHz
$\overline{FAULT}$ OUTPUT						
$\overline{FAULT}$ Output Low Voltage	V_{OL}	I_{SINK} = 500µA			0.5	V
$\overline{FAULT}$ Output High-Leakage Current					1	µA
$\overline{FAULT}$ Recovery Time	t_{FPR}	$V_{\overline{FAULT}}$ = V_{IN} (Figure 3)	6	9	11	ms
$\overline{EN}$ INPUT						
Input Logic-High	V_{IH}		1.65			V
Input Logic-Low	V_{IL}				0.5	V
Input Leakage Current	$I_{\overline{EN}}$	$V_{\overline{EN}}$ = 0V or V_{IN}			1	µA
Enable Delay Time	$t_{D_\overline{EN}}$	No load on HVBUS		10		µs
ISET INPUT						
Input Logic-High	V_{IH}		1.65			V
Input Logic-Low	V_{IL}				0.5	V
Input-Leakage Current	I_{ISET}	V_{ISET} = 0V or V_{IN}			2	µA
ESD PROTECTION (D+, D-, BUS, $\overline{EN}$, $\overline{FAULT}$, IN, ISET)						
ESD Protection Level	V_{ESD}	Human Body Model		±2		kV
ESD PROTECTION (HVD+, HVD-, HVBUS)						
ESD Protection Level (Note 4)	V_{ESD}	ISO 10605 Air Gap (330pF, 2kΩ)		±25		kV
		ISO 10605 Contact (330pF, 2kΩ)		±8		
		IEC 61000-4-2 Air Gap (150pF, 330Ω)		±25		
		IEC 61000-4-2 Contact (150pF, 330Ω)		±8		

Note 1: Specifications with minimum and maximum limits are 100% production tested at T_A = +25°C and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.
Note 2: Forward current is defined as current into BUS and out of HVBUS. See the *Functional Diagram*.
Note 3: Guaranteed by design. Limits are not production tested.
Note 4: Tested in the *Typical Application Circuit*, as shown on the evaluation kit.

Timing Diagrams/Test Circuits

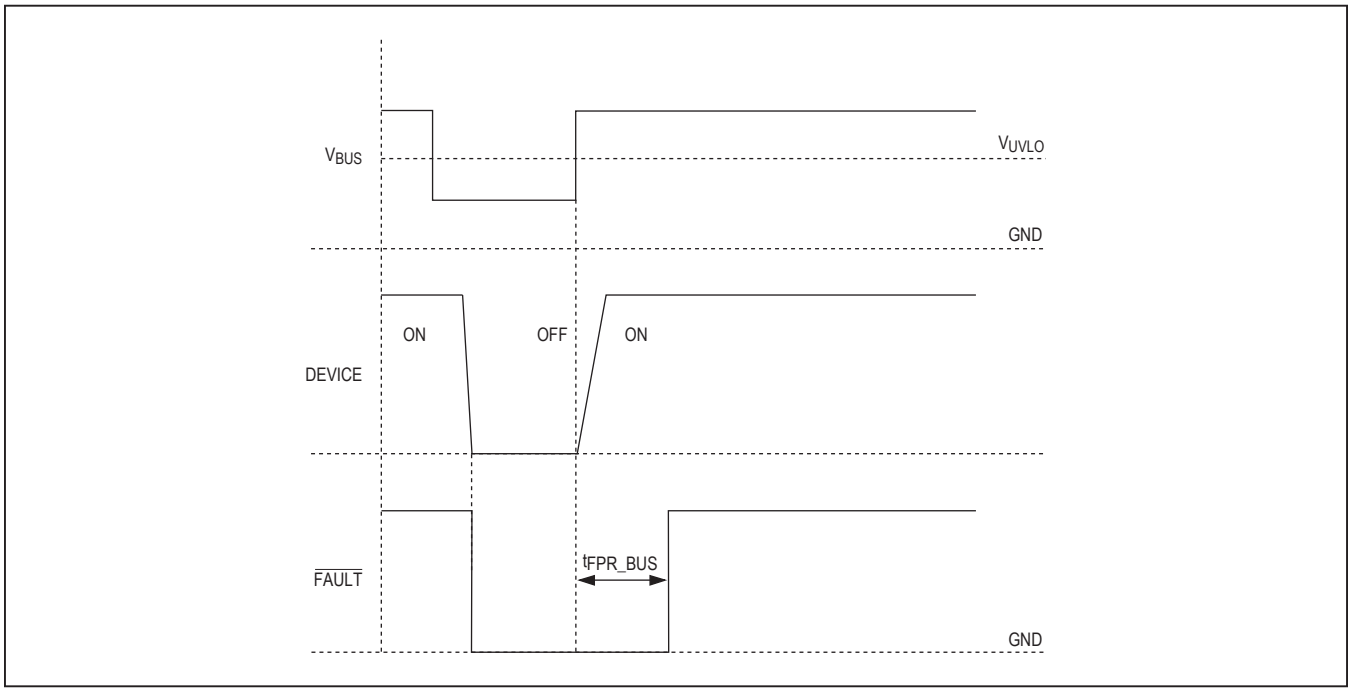


Figure 1. Timing Diagram for Undervoltage Lockout on BUS

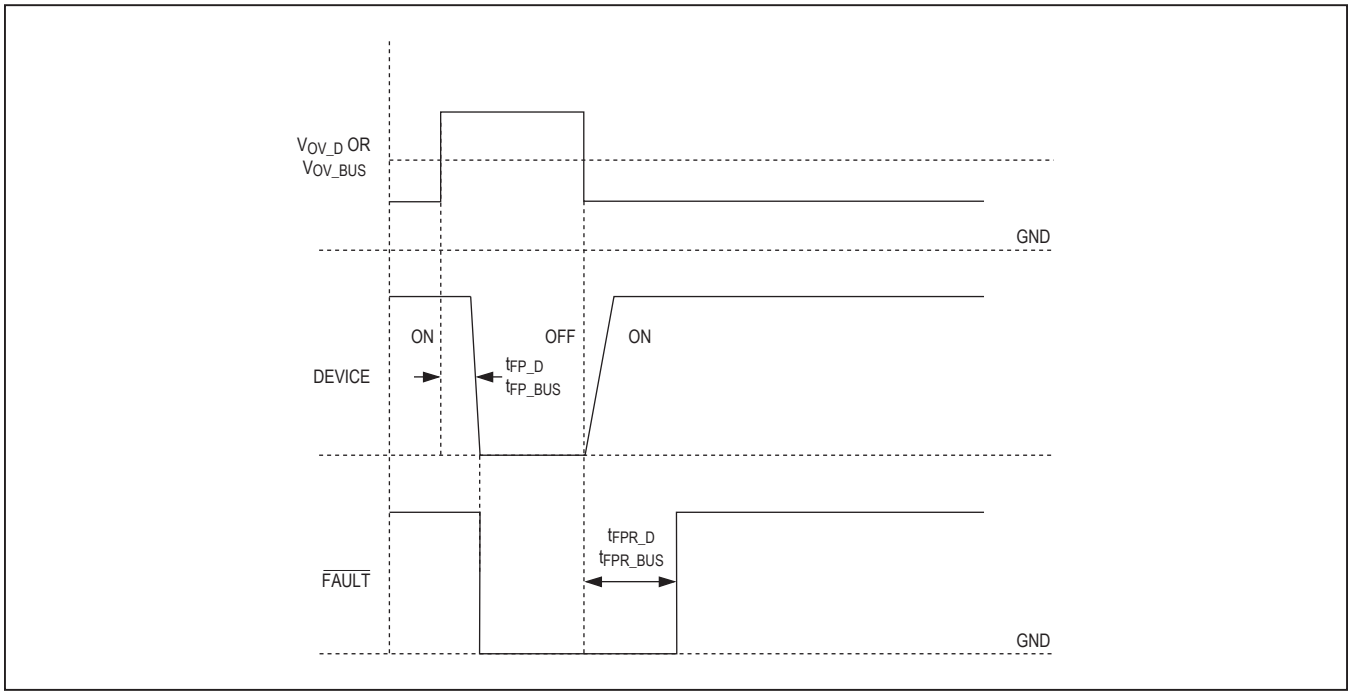


Figure 2. Timing Diagram for Overvoltage Protection on HVBUS, HVD+, and HVD-

Timing Diagrams/Test Circuits (continued)

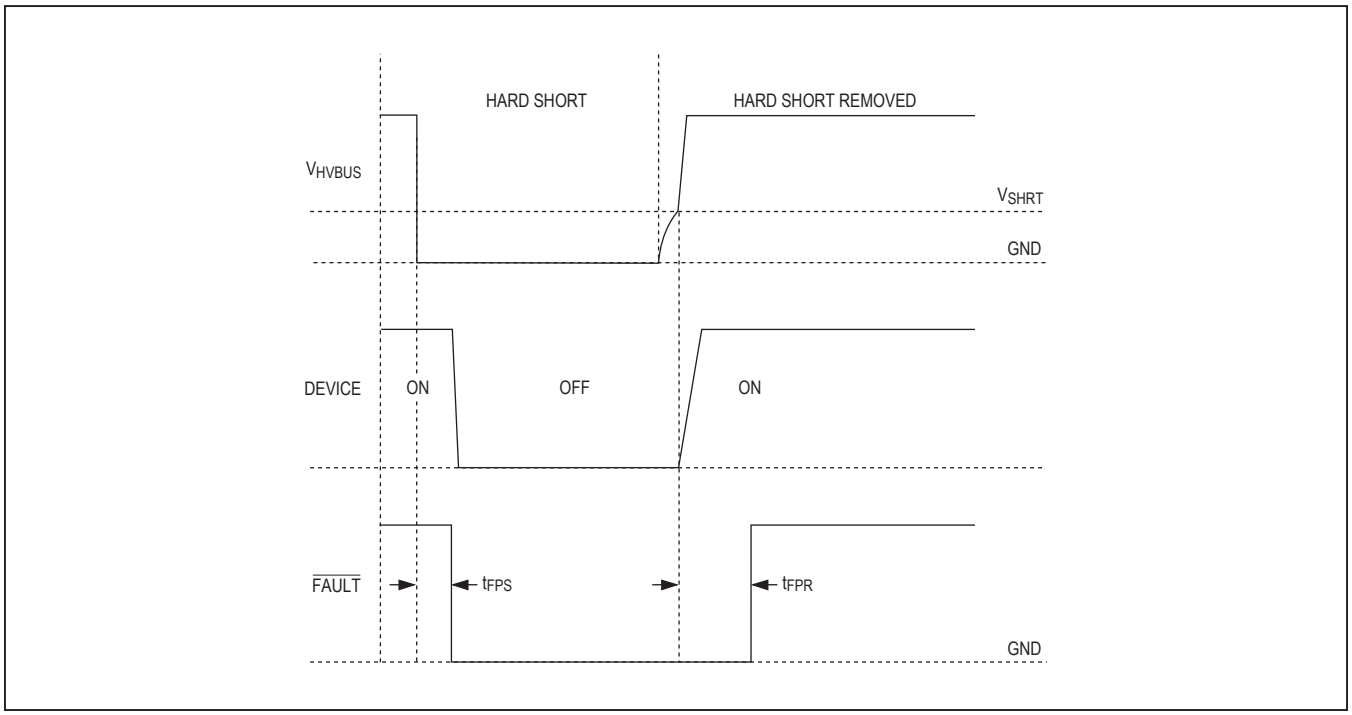


Figure 3. Timing Diagram for Short-to-Ground Protection

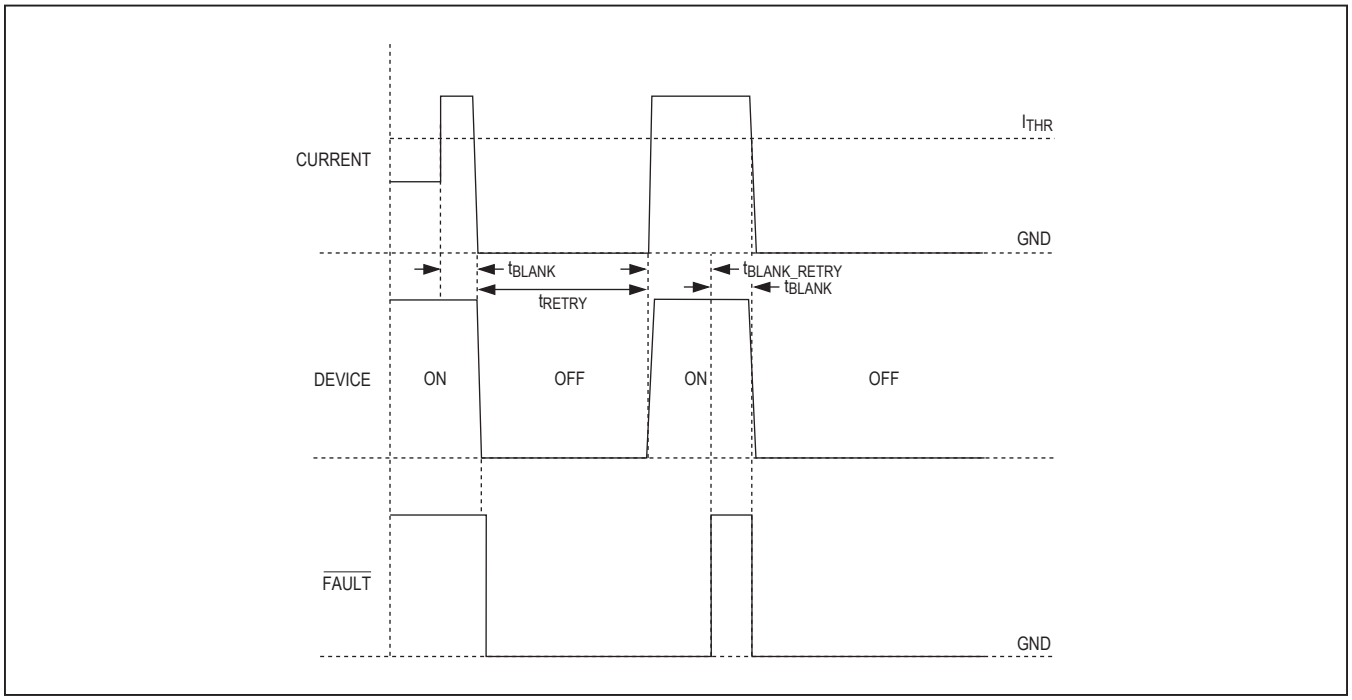


Figure 4. Timing Diagram for Overcurrent Protection

Timing Diagrams/Test Circuits (continued)

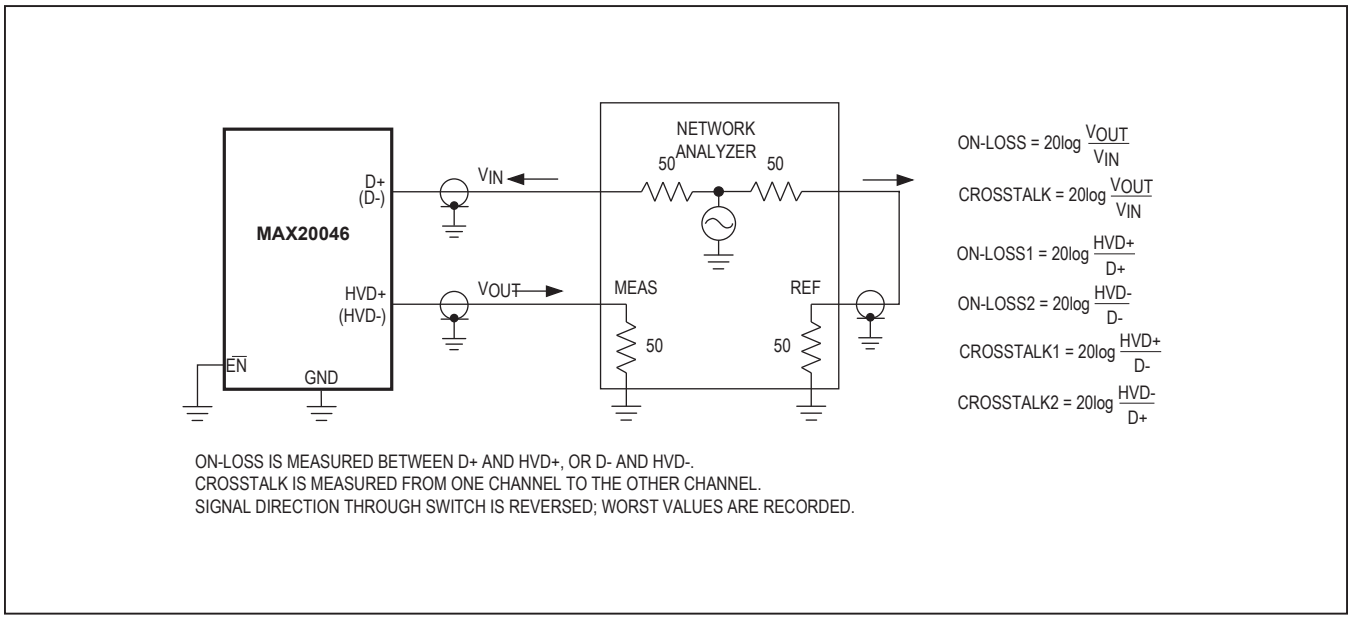


Figure 5. On-Channel -3dB Bandwidth and Crosstalk

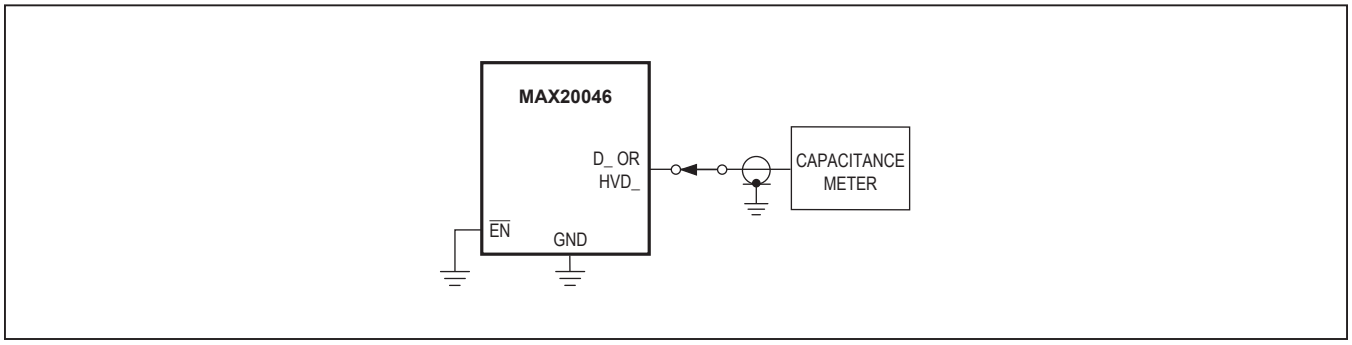


Figure 6. On-Capacitance

Timing Diagrams/Test Circuits (continued)

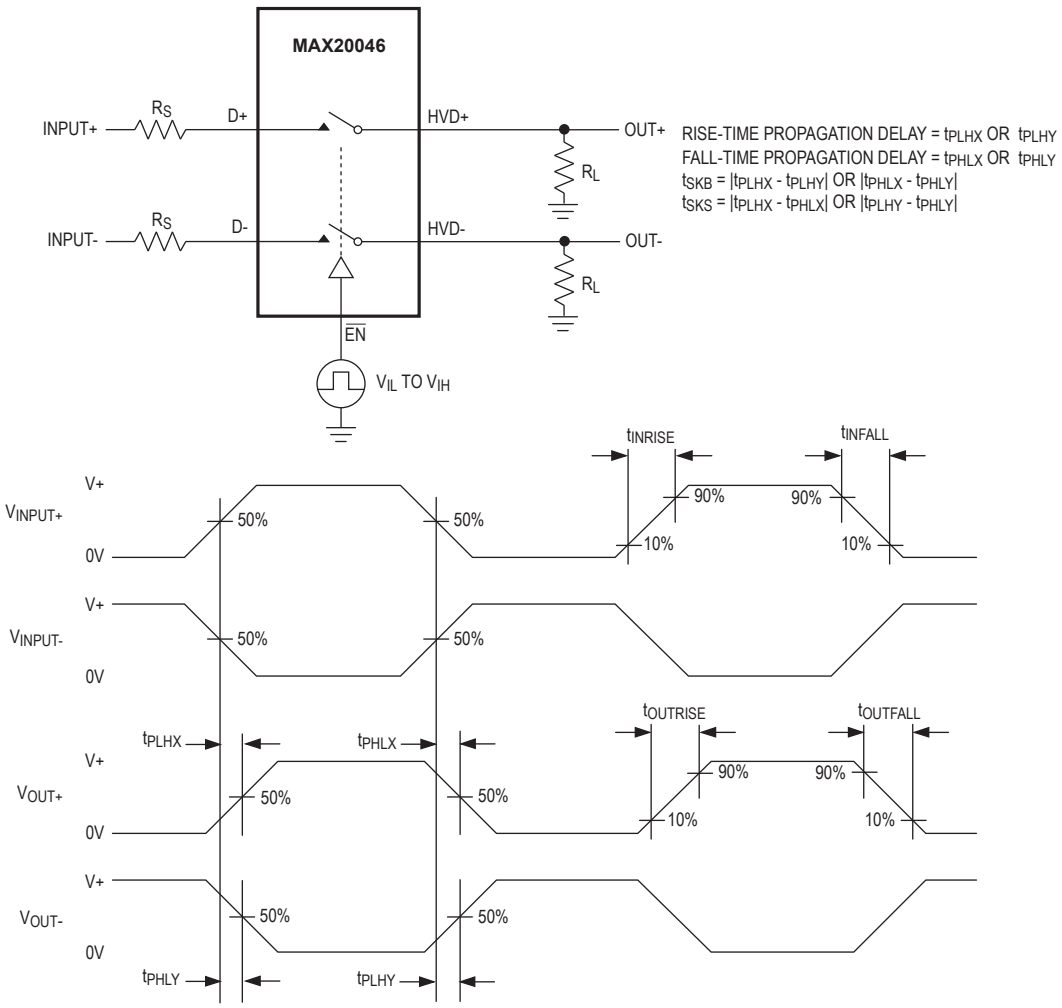
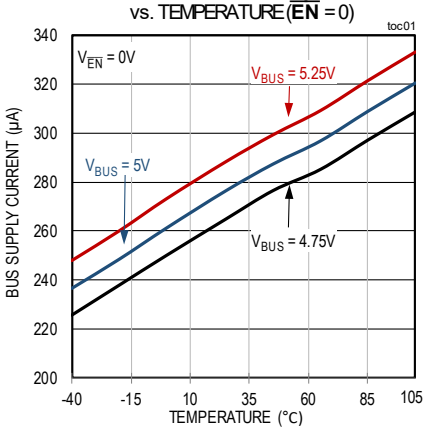


Figure 7. Propagation Delay and Output Skew

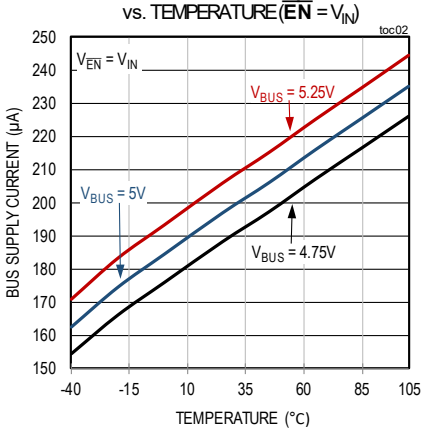
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

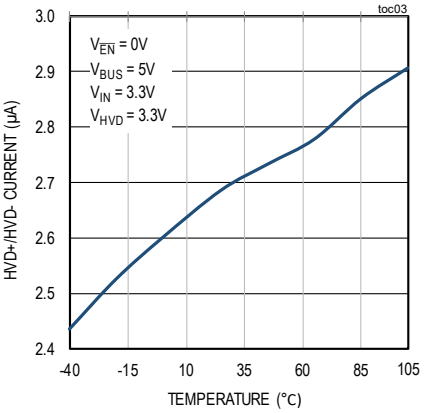
BUS SUPPLY CURRENT vs. TEMPERATURE ($\overline{EN}$ = 0)



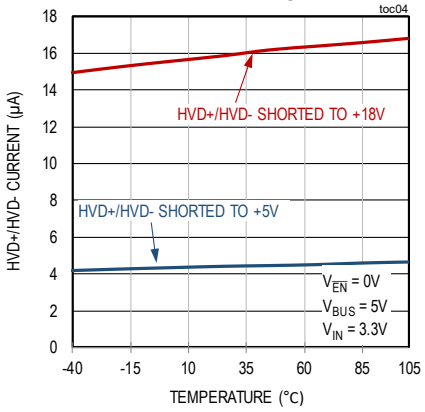
BUS SUPPLY CURRENT vs. TEMPERATURE ($\overline{EN}$ = V_{IN})



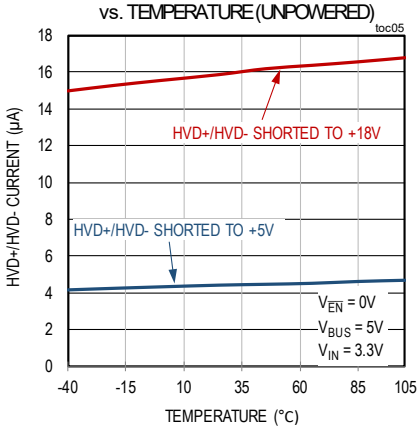
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



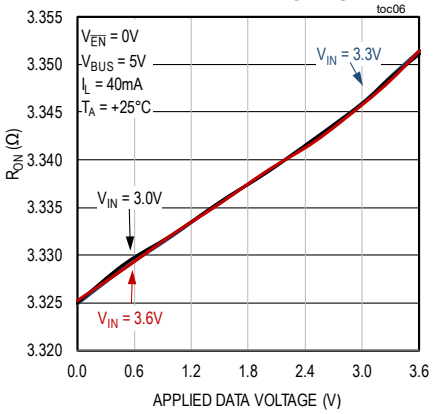
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



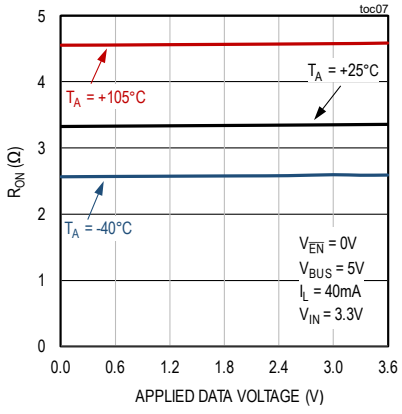
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE (UNPOWERED)



DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



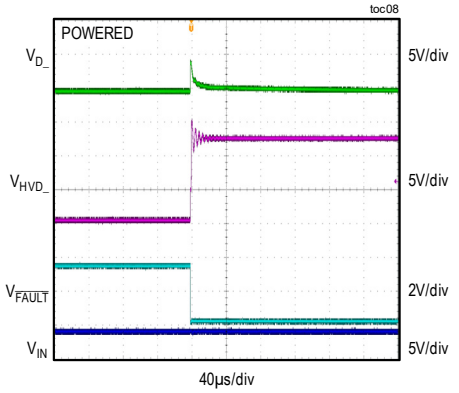
DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



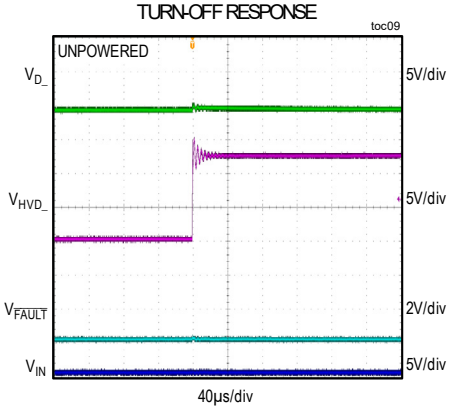
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

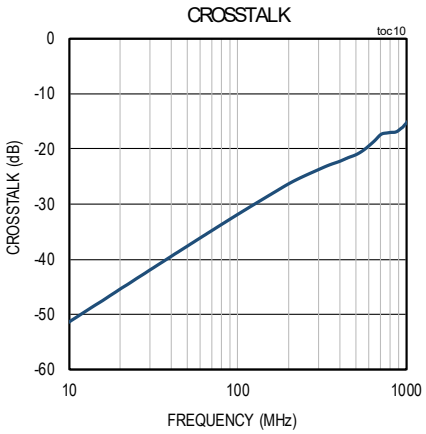
HVD+/HVD- SHORT-TO-BATTERY TURN-OFF RESPONSE



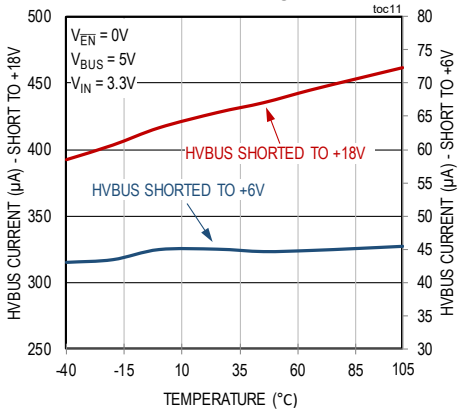
HVD+/HVD- SHORT-TO-BATTERY TURN-OFF RESPONSE



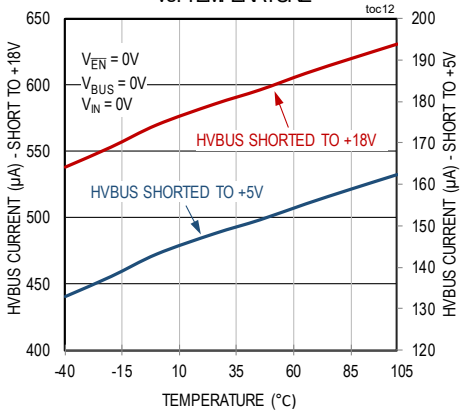
CROSSTALK



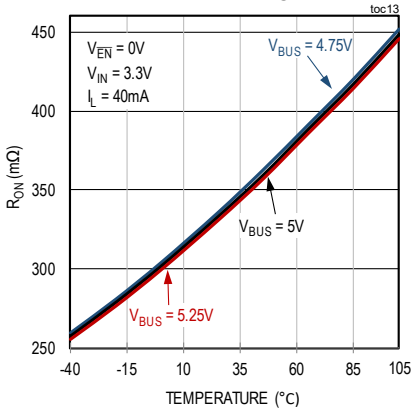
HVBUS LEAKAGE CURRENT vs. TEMPERATURE



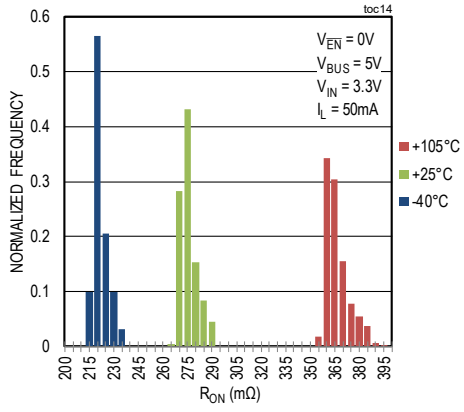
HVBUS LEAKAGE CURRENT vs. TEMPERATURE



BUS ON-RESISTANCE vs. TEMPERATURE



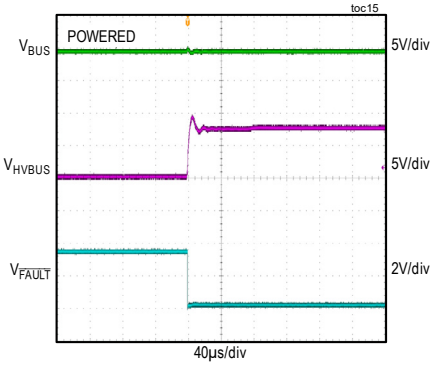
BUS ON-RESISTANCE HISTOGRAM



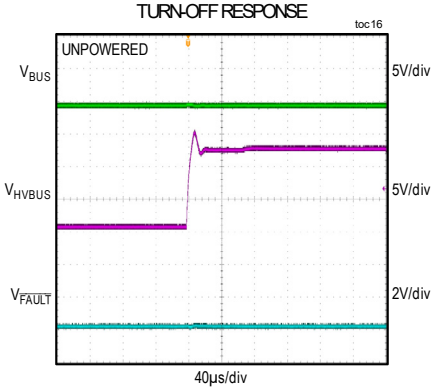
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

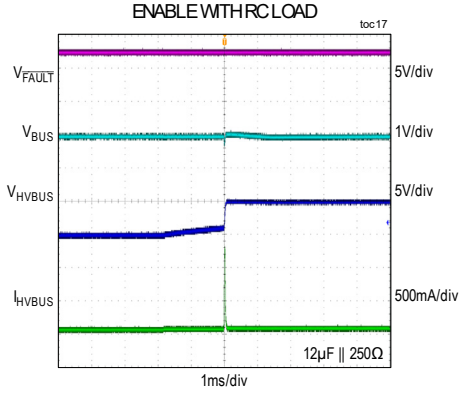
HVBUS SHORT-TO-BATTERY TURN-OFF RESPONSE



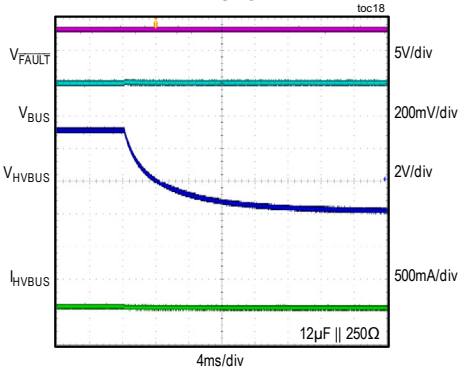
HVBUS SHORT-TO-BATTERY TURN-OFF RESPONSE



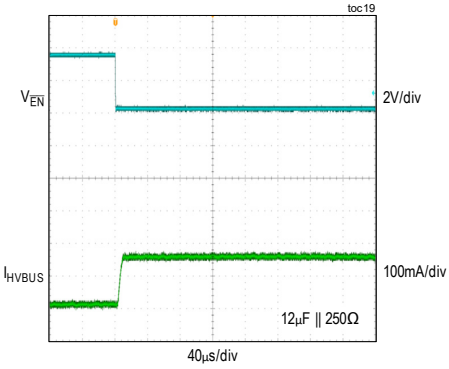
INRUSH CURRENT ENABLE WITH RC LOAD



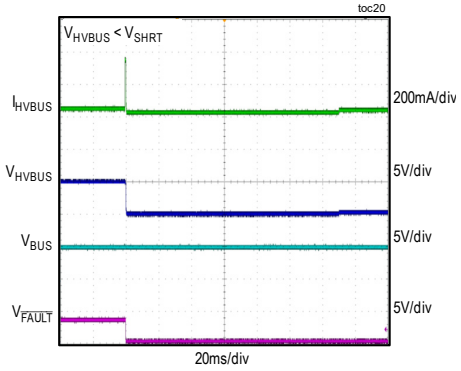
TURN-OFF RESPONSE WITH RC LOAD



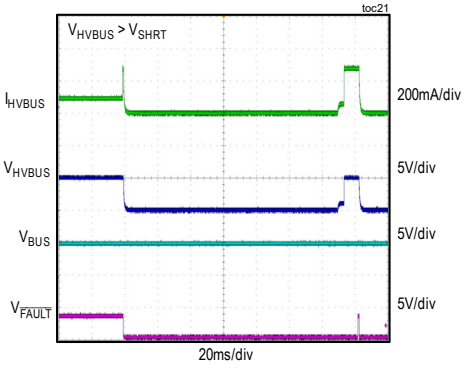
SHORT-CIRCUIT CURRENT ENABLED INTO SHORT-TO-GROUND



HVBUS OVERCURRENT AUTORETRY RESPONSE



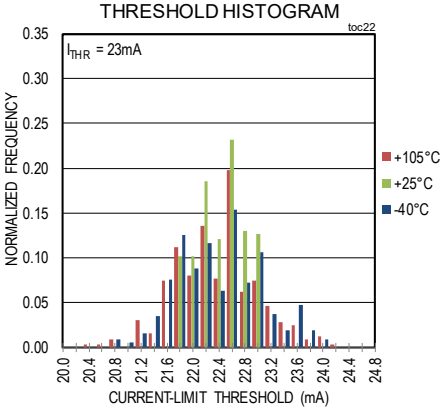
HVBUS OVERCURRENT AUTORETRY RESPONSE



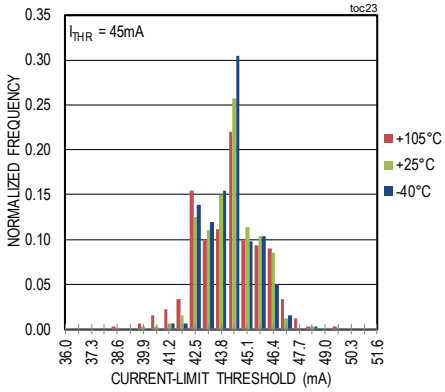
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

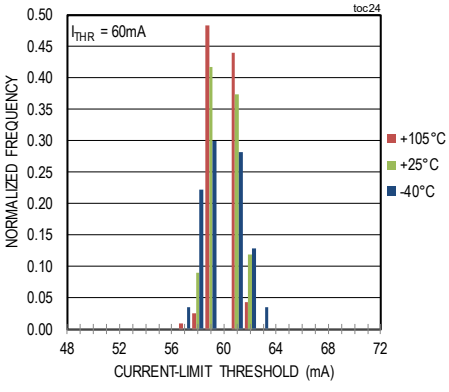
MAX20046 CURRENT-THRESHOLD HISTOGRAM



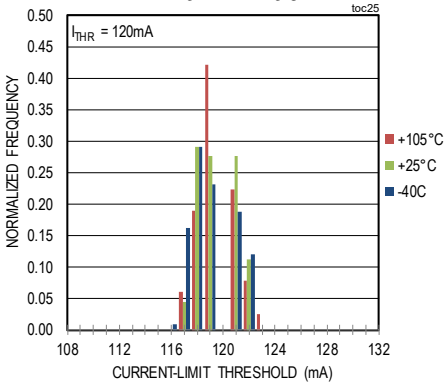
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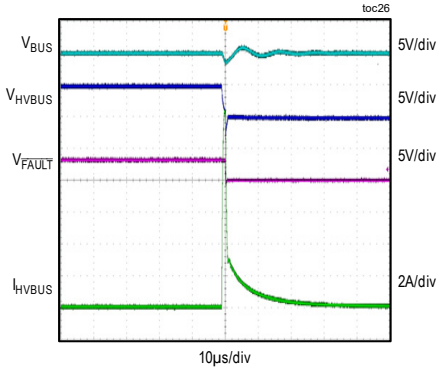
MAX20046 CURRENT-THRESHOLD HISTOGRAM



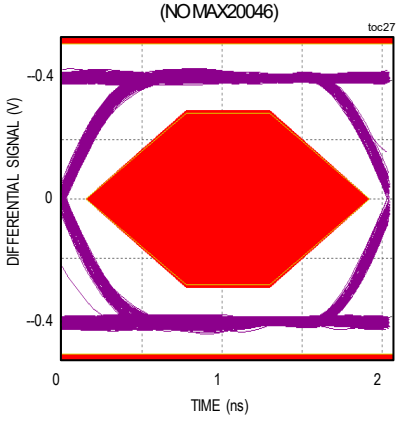
MAX20046 CURRENT THRESHOLD HISTOGRAM



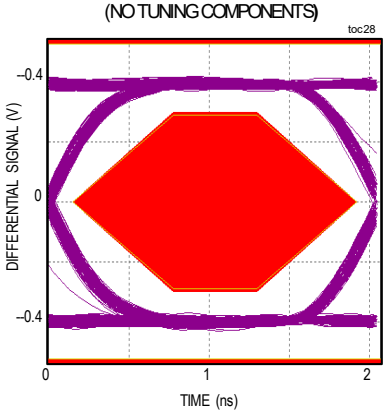
HVBUS INRUSH CURRENT FOR SHORT-TO-GROUND RESPONSE



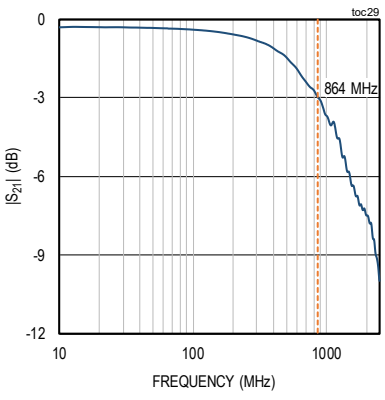
REFERENCE HIGH-SPEED EYE DIAGRAM (NO MAX20046)



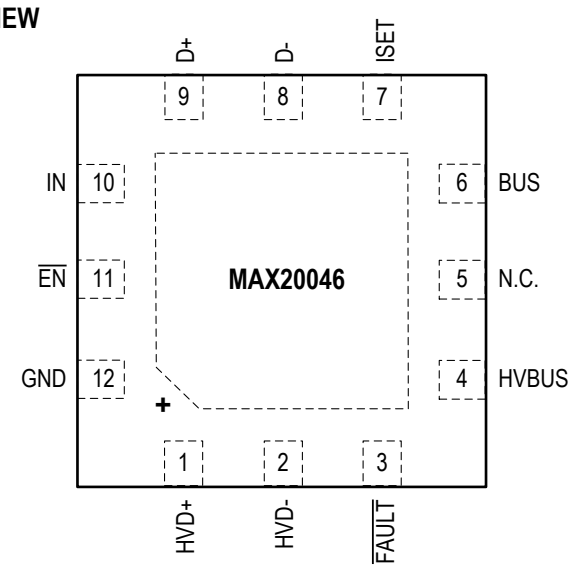
USB 2.0 HIGH-SPEED EYE DIAGRAM (NO TUNING COMPONENTS)



SINGLE-ENDED BANDWIDTH



Pin Configuration



TQFN / SW TQFN
3mm x 3mm

Pin Description

PIN	NAME	DESCRIPTION
1	HVD+	High-Voltage-Protected USB Differential Data D+ Output. Connect HVD+ directly to USB connector D+.
2	HVD-	High-Voltage-Protected USB Differential Data D- Output. Connect HVD- directly to USB connector D-.
3	$\overline{\text{FAULT}}$	Open-Drain Fault-Indicator Output. Indicates if any of the following fault conditions exist: overvoltage on HVD-, HVD+, or HVBUS; overcurrent on HVBUS; short-to-GND on HVBUS; UVLO on V_{BUS}; or overtemperature.
4	HVBUS	Protected BUS Output. Connect HVBUS directly to the USB connector. Connect 0.1µF capacitor and a 1Ω resistor in series with a 10µF capacitor from HVBUS to GND.
5	N.C.	No Connection. Internally connected to IC ground.
6	BUS	USB Power Supply. Connect BUS to USB +5V supply. Connect a 0.1µF and a 10µF, low-ESR ceramic capacitor from BUS to GND.
7	ISET	HVBUS Current-Limit-Setting Pin. Connect ISET to GND or 3.3V based on the desired current limit, as outlined in the *Electrical Characteristics* table.
8	D-	USB Differential Data D- Input. Connect D- to low-voltage USB transceiver D-.
9	D+	USB Differential Data D+ Input. Connect D+ to low-voltage USB transceiver D+.
10	IN	Logic Power-Supply Input. The supply voltage range is from +3.0V to +3.6V. Bypass IN to GND with a 10µF ceramic capacitor.
11	$\overline{\text{EN}}$	Active-Low Enable Input. Drive $\overline{\text{EN}}$ low to enable the BUS power switch.
12	GND	Ground

Detailed Description

The MAX20046 device provides high-ESD and short-circuit protection for the USB data and USB power line in automotive radio, navigation, connectivity, and USB hub applications. The device supports USB Hi-Speed (480Mbps), USB full-speed (12Mbps), and USB low-speed (1.5Mbps) operation.

The short-circuit protection features include short-to-battery on the protected HVBUS, as well as short-to-HVBUS and short-to-battery on the protected HVD+ and HVD-. Short-to-GND and overcurrent protection are also provided on the protected HVBUS output to protect the internal BUS power rail from overcurrent faults.

The device features high-ESD protection to ±25kV Air Gap Discharge and ±8kV Contact Discharge on all protected HVBUS, HVD+, and HVD- outputs.

The device features a 500mΩ (max) USB power switch and two low on-resistance (R_{ON}), USB 2.0 switches. This device also features an enable input, fault output, 9ms fault-recovery time, 1ms overcurrent blanking time, and integrated overcurrent autoretry.

BUS Undervoltage Lockout (Power-On Reset)

The device has a 4.2V (typ) undervoltage-lockout threshold (V_{UVLO}). When V_{BUS} is less than V_{UVLO}, $\overline{FAULT}$ is enabled and all the device switches are high impedance.

HVBUS Overvoltage Protection

The device has a fixed 5.7V (typ) HVBUS protection trip threshold; when HVBUS rises from V_{BUS} to > 5.7V, the device is turned off. Connect a RC snubber network from HVBUS to GND to limit positive inductive-voltage spikes that are caused by inductance from long wires at turn-off.

HVBUS Short-to-Ground

The device has a short-to-ground threshold (V_{SHRT}). When HVBUS falls below the V_{SHRT} threshold, the main power switch is turned off. During continuous short-to-ground conditions, a small autoreset current remains active to detect removal of the short circuit.

HVBUS Overcurrent Protection

The device has GPIO selectable forward-current threshold (I_{THR}). When the HVBUS forward current exceeds I_{THR}, the device is turned off. Connect the ISET pin to GND or 3.3V to set the desired current limit, as shown in the *Electrical Characteristics* table. Forward current is defined as current into BUS and out of HVBUS. See the *Functional Diagram*.

HVD+ and HVD- Overvoltage Protection

The device has a 3.9V (max) overvoltage threshold (V_{OV_D}). When HVD+ or HVD- is greater than V_{OV_D}, $\overline{FAULT}$ asserts low and all the device switches are high impedance. Note that HVD+ and HVD- do not have short-to-ground protection. Forward current is limited by the upstream transceiver.

$\overline{FAULT}$ Output

FAULT goes low when a fault is detected on HVD+, HVD-, or HVBUS. $\overline{FAULT}$ indicates if any of the following conditions exist: overvoltage on HVD-, HVD+, or HVBUS; overcurrent on HVBUS; short-to-GND on HVBUS; UVLO on VBUS; or overtemperature. All USB switches are turned off in the event of a fault, except for short-to-ground fault on HVBUS in which case the data switches remain active for OTG compatibility. Connect a 100kΩ pullup resistor from $\overline{FAULT}$ to IN.

$\overline{EN}$ Input

$\overline{EN}$ is an active-low enable input. Drive $\overline{EN}$ low to enable the BUS protection switch and allow for normal operation.

The MAX20046 device supports USB OTG. Disabling the device through the $\overline{EN}$ pin disables the +5V BUS power switch, but leaves the D+ and D- data switches closed. This allows for a downstream device to assume the role of host when negotiated per the USB Host Negotiation Protocol. In this mode, the HVBUS, HVD+, and HVD- outputs continue to be protected and $\overline{FAULT}$ continues to assert normally in response to overvoltage conditions on these pins.

Applications Information

Power-Supply Bypass Capacitor

Connect a 1Ω resistor in series with a 10µF capacitor from HVBUS to GND to avoid overshoots. Bypass HVBUS to GND with a 0.1µF ceramic capacitor as close as possible to the device to provide ±2kV (HBM) ESD protection on the pin. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent violation of the +6V absolute maximum rating on BUS. Connect a 10µF low-ESR ceramic capacitor from BUS to GND. Connect a 10µF ceramic capacitor from IN to GND. Place these components on the same plane as the IC, close to the IN and GND pins.

Layout of USB Data Line Traces

USB Hi-Speed requires careful PCB layout with 90Ω controlled-impedance matched traces of equal lengths. Use LC tuning components on the data lines, as shown in the *Typical Operating Circuit*. The values of these components are layout and captive-cable dependent. Contact Maxim technical support for more detailed information.

±25kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The device has extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect against ESD of ±25kV at the HVD+, HVD-, and HVBUS ports without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the device keeps working without latchup, whereas other solutions can latch and must be powered down to remove latchup. ESD protection can be tested in various ways; this product is characterized for protection to the following limits:

- ±2kV using the Human Body Model
- ±25kV using IEC 61000-4-2's Air-Gap Discharge method, EN = GND
- ±8kV using the Contact Discharge method specified in IEC 61000-4-2, EN = GND

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 8 shows the Human Body Model, and Figure 9 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The MAX20046 helps users design equipment that meets Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 10), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 11 shows the current waveform for the ±8kV, IEC 61000-4-2 Level 4, ESD Contact Discharge test. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

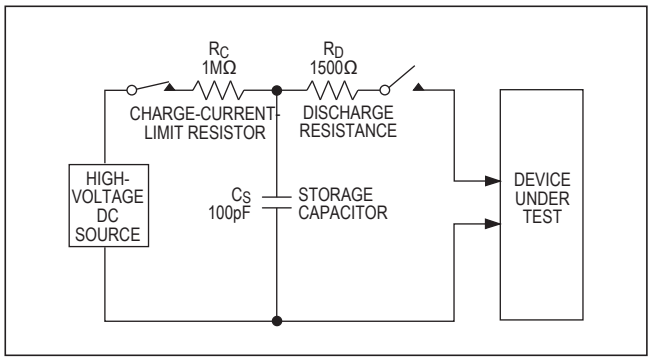


Figure 8. Human Body ESD Test Model

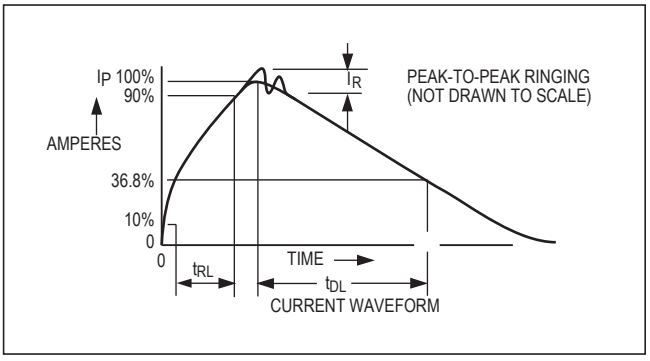


Figure 9. Human Body Current Waveform

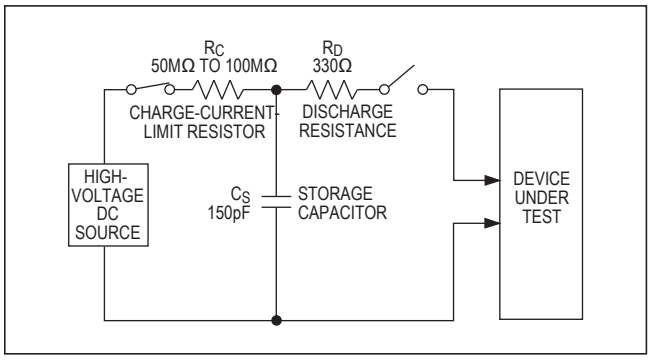


Figure 10. IEC 61000-4-2 ESD Test Model

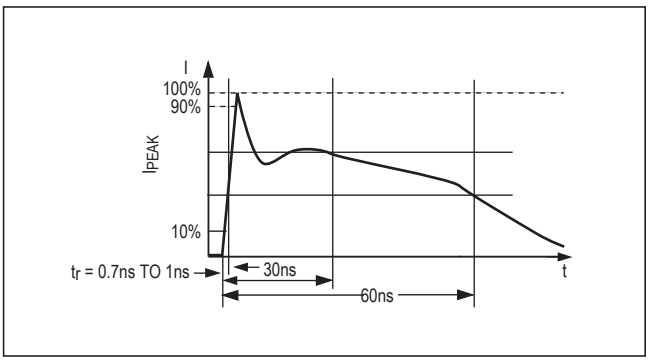
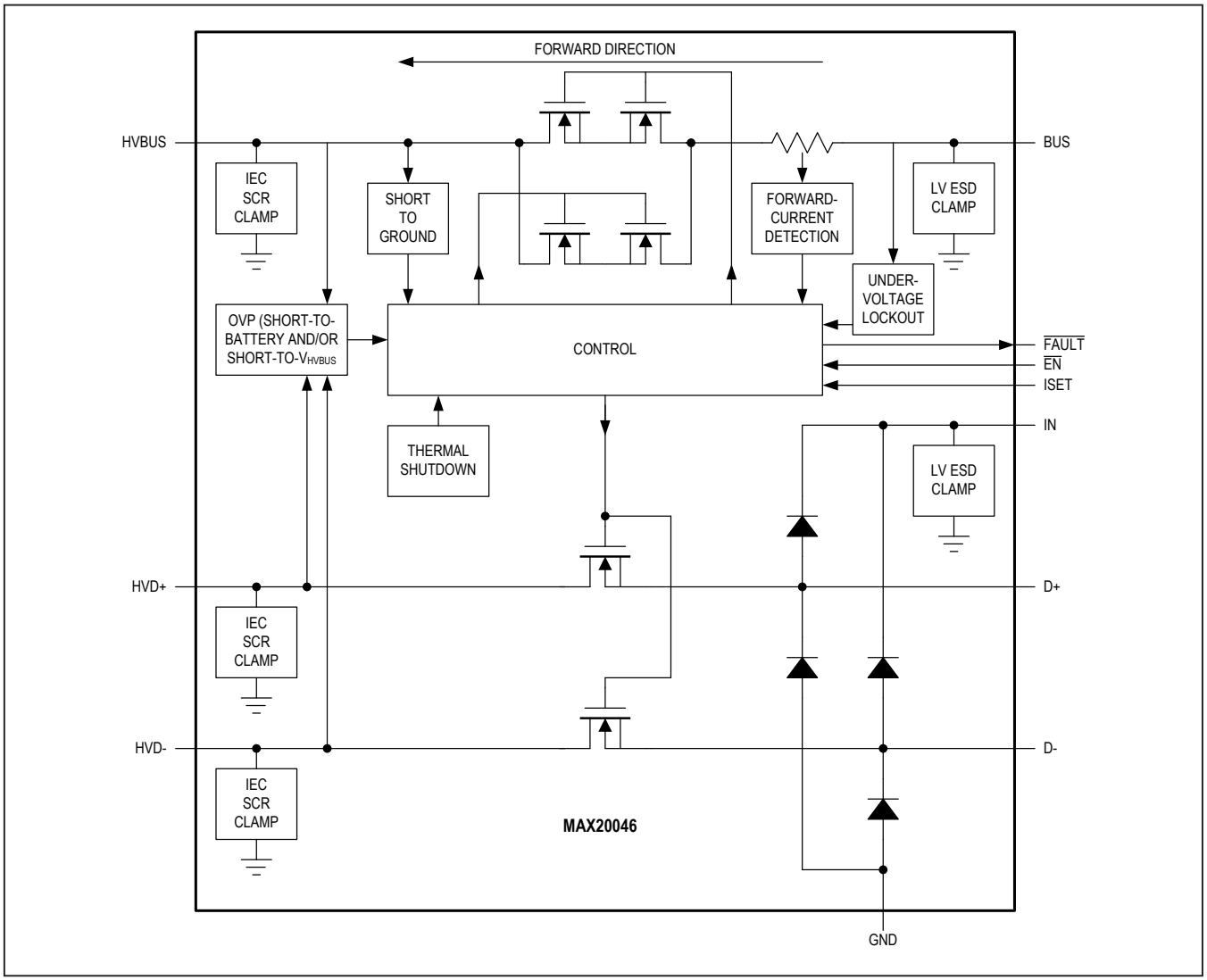


Figure 11. IEC 61000-4-2 ESD Generator Current Waveform

Functional Diagram



Ordering Information

PART	TEMP RANGE	DESCRIPTION	PIN-PACKAGE
MAX20046GTCA/V+	-40°C to +105°C	GPIO-selectable 23/45mA current limits	12 TQFN-EP*
MAX20046GTCA/V+T	-40°C to +105°C	GPIO-selectable 23/45mA current limits	12 TQFN-EP*
MAX20046GTC/V+	-40°C to +105°C	GPIO-selectable 60/120mA current limits	12 TQFN-EP*
MAX20046GTC/V+T	-40°C to +105°C	GPIO-selectable 60/120mA current limits	12 TQFN-EP*
MAX20046GTCA/VY+	-40°C to +105°C	GPIO-selectable 23/45mA current limits	12 SW TQFN-EP*
MAX20046GTCA/VY+T	-40°C to +105°C	GPIO-selectable 23/45mA current limits	12 SW TQFN-EP*
MAX20046GTC/VY+	-40°C to +105°C	GPIO-selectable 60/120mA current limits	12 SW TQFN-EP*
MAX20046GTC/VY+T	-40°C to +105°C	GPIO-selectable 60/120mA current limits	12 SW TQFN-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.
Y = Side-wettable package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/17	Initial release	—
1	718	Updated *Package Information* table, *Pin Configuration*, and *Ordering Information* table.	2, 13, 17

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